REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	8/12/97	6/15/93-6/14/96

4. TITLE AND SUBTITLE
Single Electron And Quantum Effects
In Semiconductor Nanodevices

5. FUNDING NUMBERS
N/N00014-93-1-0882

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9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Office of Naval Research
800 North Quincy Street
Arlington, Virginia 22217-5660

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
The views, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an offical Department of the Navy position, policy or decision, unless designated by other documentation.

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12 b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

Under the support of the grant, we have (1) developed a variety of sub-20 nm nanofabrication techniques; (2) proposed and demonstrated a new field induced quantum dot transistor (QDTs), and observed conductance oscillations, the interplay between quantum and Coulomb effects, and oscillation peak splitting; (3) proposed and demonstrated two quantum wave bandstop filters; (4) demonstrated the first Si single-electron transistors and achieved record operation temperature; (5) demonstrated the first single hole transistors; and (6) modeled and simulated the operation of Si QDTs, quantum effects, Coulomb effects, and many-body effects.

14. SUBJECT TERMS	15. NUMBER IF PAGES
single electron transistor, quantum dots, nanofabrication, and simulation	16. PRICE CODE

17. SECURITY CLASSIFICATION OR REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

SINGLE ELECTRON AND QUANTUM EFFECTS IN SEMICONDUCTOR NANODEVICES

FINAL REPORT

STEPHEN Y. CHOU AND PAUL P. RUDEN

AUGUST 27, 1996

DEFENSE ADVANCED RESEARCH PROGRAM AGENCY

THROUGH

OFFICE OF NAVAL RESEARCH

CONTRACT/GRANT NUMBER N/N00014-93-1-0882

DEPARTMENT OF ELECTRICAL ENGINEERING
UNIVERSITY OF MINNESOTA
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I. Objective

To experimentally and theoretically explore innovative nanoscale transistors, quantum effects and single electron effects, and their applications in ultra-high density circuits and memories.

II. Summary of Major Accomplishments

2.1. Sub-20 nm Nanofabrication

To fabricate the innovative nanoscale transistors needed for our investigation, we first developed a variety of sub-20 nm nanobrication techniques[1,2]. They include an enhanced ultra-high resolution electron beam lithography, improved RIE recipes, and a size reduction process by oxidation.

2.2. Field Induced Quantum-dot Transistor

We proposed and fabricated a new field induced quantum dot transistor (QDT). The gates are fabricated on top of a d-doped AlGaAs/GaAs heterostructure using electron-beam lithography and a lift-off process[3,4]. The most important feature of the QDT is a positive-biased dot gate, which, sandwiched between two split-gates, creates a much smaller quantum-dot and better confinement, leading to the observation of conductance oscillation at 40K (a record temperature for QDTs in III-V compounds semiconductors) and the interplay between quantum effects and Coulomb effects (previously Coulomb effects dominatesin all QDTs because of a large dot size). We also observed, for the first time, peak-splitting due to the Femi-level splitting induced by a large drain bias.

2.3. Quantum Wave Bandstop Filters

We demonstrated, based on the concept of a microwave waveguide cavity bandstop filter, two quantum wave bandstop filters using field-induced nanoscale cavities[5,6]. As the Fermi level inside the quantum cavity is changed by the gate-voltage, we observed that, at certain gate-voltage, the transmission of electron waves is partially blocked and the drain current drops drastically. This current drop can be attributed to the destructive interference between different modes in the cavity. This is one of the first clear experimental evidences of quantum wave band filters.

The first type of quantum bandstop filter has a cavity created by placing a dot-gate inside the gap of a split-gate. The dot-gate has a 80 nm diameter metal dot in the middle of a 30 nm wide metal wire; when positively biased, it induces a cavity connected by two one-dimensional (1D) wires at the heterostructure interface. The negatively biased split-gate is used to control the electron population in the cavity and 1D wires. The gates are fabricated on top of a d-doped AlGaAs/GaAs heterostructure using electron-beam lithography.

The second type of quantum bandstop filter has a cavity formed by placing a straight-wire gate between a pair of U-shaped split-gates. The U-shaped split-gates create the cavity and the wire-gate controls the electron population. A similar current drop in the propagating regime has been observed. This indicates that the current notch is a general property of electron transport through a quantum cavity coupled to two 1D channels.

2.4. The First 170 K Silicon Single-Electron Quantum Dot Transistors

We have demonstrated the first silicon single electron quantum dot transistors (QDTs) that can operate at 170 K[7]. The key that led to the success is a novel fabrication process that can create a silicon dot (a size 8 nm x 30 nm x 30 nm) separated from the source and the drain by two constrictions. The silicon dot is surrounded by thermal oxide, and has a gate on top. The gate can change the charge concentration inside the dot. Since the quantum dot is small in size, discrete energy levels are formed. The single-electron quantum dot transistors show oscillation of the drain current as a function of the gate voltage at temperatures up to 170 K and drain biases up to 80 mV. The oscillation is due to electron tunneling through the discrete energy levels inside the quantum dot. The average energy level spacing is ~ 70 meV. Data analysis shows that the discrete energy levels are caused by Coulomb interactive as well as quantum size effects.

2.5. The First Single Hole quantum dot transistors

To make complementary single-charge transistor circuits, we must have single-hole transistors (SHTs)[8,9]. However, SHTs had never been demonstrated before. To achieve SHTs, we used a fabrication process siliar to those used for silicon SETs, except that the source and the drain were doped with n-type, and the gate and the drain were biased negatively. Drain current oscillation due to single tunneling was observed at a temperature up to 110 K and a drain bias up to 50 mV, giving an average hole energy level spacing of ~ 42 meV.

2.6. Modeling and Simulation

We calculated the electronic structure of III-V heterostructure based quantum dots, taking into account explicitly the electron-electron interaction within a quantum dot as well as Coulomb coupling between electrons in vertically stacked quantum dots[10-14]. We identified strong correlation effects through calculations in the framework of the configuration interaction technique. These correlation effects are expected to have considerable a impact on Coulomb blockade limited transport through quantum dots. The associated polarization effects may lend themselves to an alternative way of representing information in a quantum structure based computer. Early results obtained through variational calculations were reported at the 1993 International Semiconductor Device Research Symposium in Charlottesville, VA, December 1993. A detailed description of the results obtained within the configuration interaction technique using a two-dimensional

approximation was published in Philosophical Magazine. Subsequently we investigated Coulomb effects in three-dimensional model quantum dots. We explored the interesting regime of box dimensions that are of comparable magnitude in all three spacial directions. Our results were published in Journal of Applied Physics.

In support of the interpretation of experimental data obtained earlier under this program, we performed extensive numerical electronic structure calculations for dual gate quantum wire structures. A new method for calculating the surface potential was developed. We found that the two gates (wire gate and split gate) control the electron population and its spatial distribution with different degrees of effectiveness. The results were published in Journal of Applied Physics. We also suggested a method for independent control of the electron population and its spatial distribution in the quantum wire. This work was presented at the 1995 International Semiconductor Device Research Symposium in Charlottesville, VA, December 1995.

Recently, we started calculating the electronic structures on n-type and p-type silicon based quantum dots. The work is motivated in part by new breakthroughs in the fabrication of silicon nanostructures, which were in part achieved under this program. A manuscript of the theoretical results obtained in a single particle model is in preparation.

III. List of Publications

[1] P. B. Fischer and S. Y. Chou, "10 nm Electron Beam Lithography and sub-50 nm overlay using a modified scanning election microscope," *Appl. Phys. Lett.*, **62**(23), 2989, 1993.

[2] P. B. Fischer, and S. Y. Chou, "10 nm Si Pillars Fabricated using E-Beam Lithography, Reactive Ion Etching, and HF Etching," *J. Vac. Sci. and Tech.*,B11(6), 2524, 1993.

[3] Y. Wang and S. Y. Chou, "Planar Field Induced Quantum Dot Transistor," *Appl. Phys. Lett.*, **63**(16), 2257, 1993.

[4] Y. Wang, S. Y. Chou and M. R. Melloch, "Effects of Bias, Temperature, and Construction Potential Shape on 1D Ballistic Transport in a Planar Double-Gate Quantum Wire Transistor," *Superlattices and Microstructures*, 14(2/3), 227-230, 1993.

[5] Y. Wang and S. Y. Chou, "Quantum Wave Band Stop Filter,"*Appl. Phys. Lett.*, **65**(16), 2072-2074, 1994.

[6] Y. Wang, W. Y. Deng, and S. Y. Chou, "Electron Transport Through a Quantum Cavity,"*Superlattices and Microstructures*, **17**(2), 193-196, 1995.

[7] E. Leobandung, L. Gou, Y. Wang, and S. Y. Chou, "Observation of Quantum Effects and Coulomb Blockade in Silicon Quantum-Dot Transistors at Temperatures Over 100 K," *Appl. Phys. Lett.*, **67**(16), 2338-2340, 1995.

[8] E. Leobandung, L. Guo, and S. Y. Chou, "Single Hole Quantum Dot Transisteors in Silicon," *Appl. Phys. Lett.*, **67**(16), 2338-2340, 1995.

[9] E. Leobandung, L. Guo, and S. Y. Chou, "Single Electron and Hole Quantum Dot Transistors Operating above 110K," *J. Vac. Sci. and Tech.*, **B13**(6), 2865-2868, 1995.

[10] "Independent Control of Electron Density and Spatial Electron Distribution of Wire Gate Quantum Wire", R. Yang and P.P. Ruden, Proceedings 1995 Int'l. Semiconductor Device Research Symposium, 369,
1995.

[11] "Electronic Structure of Dual Gate Quantum Wire", R. Yang and P.P. Ruden, J. Appl. Phys. 79, 2517, 1996.

[12] "Electron-Electron Interaction in Three-Dimensional Model Quantum Box," R. Yang and P.P. Ruden, J. of Appl. Phys. 78, 1798, 1995.

[13] "Coulomb Effects between Electrons in Quantum Box Structures", R. Yang, P.P. Ruden, and D.L. Smith, Phil. Mag. B 71, 359, 1995.

[14] "Coulomb Coupling Effects in Single Electron Quantum Box Structures", R. Yang, P.P. Ruden, and D.L. Smith, Proceedings 1993 Int'l Semiconductor Device Research Symposium, 329, 1993.

IV. List of Personnel Participating The Scientific Project

Principal Investigator: Professor Stephen Chou and Professor Paul R. Ruden

Students supported:

Y. Wang

E. Leobandung

R. Yang

T.-N. Fang

V. Advanced Degrees Awarded to Personnel on the Project

M.S. Degree:

Y. Wang (MSEE 1993 and PhD 1995)

E. Leobandung (MSEE 1995)

R. Yang (MSEE 1995)

VI. Invention Disclosure

None

10 nm electron beam lithography and sub-50 nm overlay using a modified scanning electron microscope

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Ref - 1

(Received 26 October 1992; accepted for publication 17 March 1993)

Gratings of 10 nm wide metal lines 30 nm apart, and quantum transistor gates with 10 nm wide gaps over 300 nm long between two metal rectangles have been repeatedly achieved on thick GaAs substrates using a modified scanning electron microscope operated at 35 keV and liftoff of Ni/Au. Furthermore, multilevel electron beam lithography with a standard deviation (3σ) of an overlay accuracy (30 deviation) of 50 nm has been achieved using the same modified scanning electron microscope.

The desire to study the high-speed operation and quantization effects of semiconductor devices has motivated research on the fabrication of 10 nm lateral structures. For examples, lateral quantum effect devices require ultrasmall gate geometry,[1] and metal-semiconductor-metal photodetectors require extremely dense patterns of very fine interdigitated metal fingers for high performance.[2] In addition to high resolution, high overlay accuracy is another requirement in the lithography for many novel semiconductor devices. Modified scanning electron microscopes (SEMs) are an attractive tool for nanofabrication and nanodevice research due to their high resolution, high flexibility, and low cost. However, a modified SEM does not offer a direct means for high-accuracy multilevel overlay.

Previously, modified SEMs have been used to produce 10 nm wide isolated lines and gratings of 40 nm period with 12 nm linewidth on membranes,[3] as well as 10 nm wide isolated lines and gratings of 40 nm period with 10 nm linewidths on bulk GaAs substrates using a 250 keV beam exposure and chemically assisted ion beam etching with polymethyl methacrylate (PMMA) as an etch mask.[4] However, little work has been reported on ultrahigh overlay accuracy in multilevel e-beam lithography using a modified SEM.

This letter presents the study of lithographic resolution as well as overlay capability of a modified SEM operated at 35 kV. Using a liftoff technique with PMMA resists, 10 nm metal features, either isolated or periodic with periods as small as 40 nm, have been consistently achieved on bulk GaAs substrates. A liftoff process is used because it is more difficult and challenging to achieve nanostructures than etching with a PMMA etch mask. Moreover, sub-50 nm overlay accuracy has been accomplished.

In order to achieve ultrasmall structures in PMMA, the exposure of the resist by backscattered and laterally scattered electrons must be minimized. This can be accomplished by using thin resists and relatively small exposure areas. In our experiment, GaAs wafers were coated with a 45 nm thick layer of 950 K PMMA by spinning a 1.6% solution of 950 K PMMA (in chlorobenzene) at 6.0 krpm for 60 s. The samples were then baked for 12 h at 165 °C. Our e-beam lithography system consists of a modified JEOL-840A SEM with a tungsten filament gun and equipped with a magnetic beam blanking unit and electronic rotation system. The writing field can vary from 3×4 μm to 150×250 μm by selecting different magnifications of the microscope. A personal-computer controlled pattern generator is used to control the SEM. The pattern generator was designed and built in house, utilizes a commercial computer-aided design package for pattern specification, and offers a digital-to-analog converter resolution of up to 14 bits. Several measures have been taken to reduce noise from floor vibrations and electronics. High resolution exposures are performed using a field size of 34×26 μm^2, and DAC resolution of $2^{12}\times2^{12}$ pixels.

Exposures were performed with an accelerating voltage of 35 kV, and a beam diameter of about 4 nm. In order to achieve ultra-small features, a high contrast developer-resist system was used. Development was done at 23 °C using 2-ethoxyethanol:methanol (3:7) for 7 s, methanol for 10 s, and isopropanol for 30 s. The contrast of this development process for 950 K PMMA has been measured to be seven. After development, metals were deposited by e-beam evaporation. Liftoff was performed by alternately soaking in warm acetone and spraying with a pressurized acetone jet.

Both isolated and densely spaced patterns with 10 nm features have been obtained. Figure 1 shows a scanning electron micrograph of a 40 nm period grating with 10 nm linewidths on bulk GaAs. In this particular example only 3.5 nm of Ni and 4 nm of Au have been used, but liftoff is still possible with total metal thicknesses of 20 nm. The exposure dose for the grating was 0.9 nC/cm and must be carefully controlled. The exposure area is 2 $\mu m\times1.3$ μm and the liftoff was successful over the entire area. Gratings with a period smaller than 40 nm were patterned in PMMA, but did not liftoff properly.

Figure 2 shows a scanning electron micrograph of a Ni/Au (7 nm/8 nm) constricted gate for a quantum field-effect transistor with a gap of 10 nm and a gate length of 330 nm on bulk GaAs. The constricted gate was exposed with a dose of 480 $\mu C/cm^2$. This demonstrates that not only 10 nm lines but also 10 nm spaces can be achieved using a modified SEM operated at 35 kV with liftoff techniques.

To use the modified SEM to achieve high overlay accuracy, we selected a writing field size of 12×9.3 μm^2, corresponding to a SEM magnification of 10 K. The writ-

 0003-6951/93/232989-03$06.00

10 nm Si pillars fabricated using electron-beam lithography, reactive ion etching, and HF etching

Ref-2

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(Received 21 June 1993; accepted 30 July 1993)

This article reports the fabrication and preliminary photoluminescence (PL) study of free-standing Si pillars with diameters of about 10 nm and aspect ratios greater than 15. The pillars were fabricated using electron-beam lithography, chlorine based reactive ion etching (RIE), and subsequent HF wet etching. Using HF etching offers several advantages: (a) it is a relatively stress independent process and therefore preserves the original shape of the structure; (b) it is a room temperature process; (c) it has a very controllable etch rate, ~1.9 nm/h; and (d) it can remove RIE damage and passivate the Si surface. PL with a peak at 720 nm was repeatedly observed from an array of nanoscale pillars with ~20 nm diameters. However, the cause of such PL is still unclear.

I. INTRODUCTION

The ability to fabricate nanoscale pillars in Si in a very controllable way is of great interest to many fields, such as quantum effect Si devices, nanoscale sensors, and field emitters, just to name a few. Another attractive aspect of such fabrication is the possibility to shed light on the origin of photoluminescence (PL) from porous Si.[1] To date, the PL has been explained in terms of quantum confinement,[2] and surface chemistry.[3]

Previously, oxidation techniques have been employed to further reduce the size of silicon pillars for fabricating field emitters and microsensors,[4] and for studying luminescence.[5] The oxidation process has two drawbacks. First, it is a stress dependent process, therefore is nonuniform and significantly changes the original shape of the pillars. Second, it is a high temperature process which could pose problems in some applications.

In this article we present a different approach to fabricating free-standing Si pillars with diameters of about 10 nm and aspect ratios greater than 15. The process utilizes electron beam lithography, chlorine-based reactive ion etching (RIE), and subsequent HF wet etching. HF etching offers several advantages. First, HF etching is a relatively stress independent process and therefore preserves the original shape of the structure. Second, it is a room temperature process, making it a much more versatile process than high temperature oxidation. Third, it has a very controllable etch rate, ~1.9 nm/h. And finally, it can remove RIE damage and passivate the Si surface. A preliminary investigation of PL from the nanoscale Si pillars is also presented.

II. FABRICATION

The 10 nm Si pillar fabrication process consists of three main steps: etch mask definition, RIE, and HF etching to reduce the size of the pillars. All experiments were performed on 3–12 Ω cm *p*-type (100) Si wafers. The Cr etch masks were defined using electron beam lithography and a lift-off process. Electron-beam lithography was performed using a modified scanning electron microscope (SEM), described elsewhere,[6] operated at 35 kV. Arrays of dots were exposed in 950 K polymethylmethacrylate (PMMA), 70 nm thick on top of the Si substrate, and developed in a mixture of 2-ethoxyethanol and methanol. After development, 40 nm of Cr was evaporated onto the samples. A lift-off process left arrays of Cr dots which were used as the etch mask for RIE. Figure 1 shows Cr dots with 25 nm diam and 25 nm spacings on a bulk semiconductor substrate. In our experiment a variety of samples with different pitch size and areas were used for different purposes, as discussed later.

Chlorine-based RIE was used to transform sub-50 nm-diam Cr dot patterns into Si pillars. The etching was performed in a parallel plate RIE system operated at 13.56 MHz, with Cl_2 and $SiCl_4$ flow rates of 55 and 10 sccm, respectively, a power density of 0.32 W/cm^2, a pressure of 40 mTorr and a self-bias of −85 V. The etch rate of Si was 150 nm/min. The high selectivity of the chlorine RIE process is high, approximately 40:1 (Si/Cr), therefore insuring a minimal change in mask geometry during etching. Sub-50 nm diam pillars, 500 nm tall and with near vertical sidewalls, were routinely obtained. Figure 2 shows typical etched Si pillars with the chrome masks still in place. Such 3×3 arrays of pillars of a 150 nm period were patterned to calibrate the three steps of the pillar sculpting process. The chrome masks were later chemically removed using a wet etch (Cyantek Cr-7s).

The last step of the fabrication process utilizes aqueous HF acid etching (49%) to further reduce the size of the pillars and passivate the Si surface.[7]

III. FABRICATION RESULTS AND DISCUSSION

The effect of HF etching on pillar geometry was systematically studied. Figure 3 shows scanning electron micrographs of pillars at different stages of the etching process. Figure 3(a) shows a pillar just after RIE with the Cr mask still in place but before any HF etching. The pillar is approximately 45 nm in diameter and about 450 nm tall. The top of the pillar widens slightly due to sidewall deposition during RIE which has been observed before and can be

Planar field-induced quantum dot transistor

Ref-3

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(Received 25 May 1993; accepted for publication 11 August 1993)

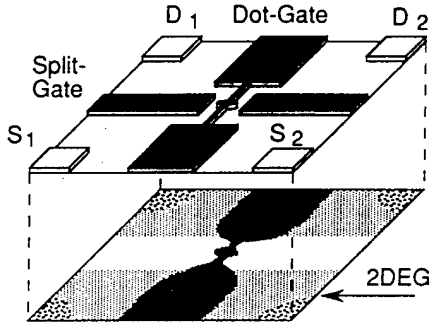
We propose and demonstrate a new field-induced quantum dot transistor that has a nanoscale dot-gate inside the gap of a split gate. Because of the novel structure and small dot size, strong oscillations in the drain current as a function of the gate bias were observed at a temperature up to 4.2 K or with a drain bias up to 5 mV. Temperature dependent study showed that the energy gaps in the dot are as large as 4.5 meV. Simulation indicates that, in the device, quantum size effect and Coulomb effect are comparable; both contribute significantly to the energy gaps in the quantum dot.

Semiconductor quantum-dot transistors are of great importance to fundamental understanding of electron transport in nanostructures and to future development of microelectronics.[1,2] Previously, transistors based on the transport through a three-dimensionally confined potential box (so-called dot) induced by the field effect of gate electrodes were studied.[3–6] Although these transistors are commonly called quantum-dot transistors (QDTs), it is the classical Coulomb energy levels, not quantum energy levels, in the box that are responsible for the observed drain current oscillations. This is because the typical dot size of these transistors is much larger than 0.1 μm, making quantization energy much smaller than Coulomb energy. In this letter, we propose and demonstrate a field-induced QDT with a new gate structure, and show that both quantum effect and Coulomb effect are important to the energy levels in this QDT.

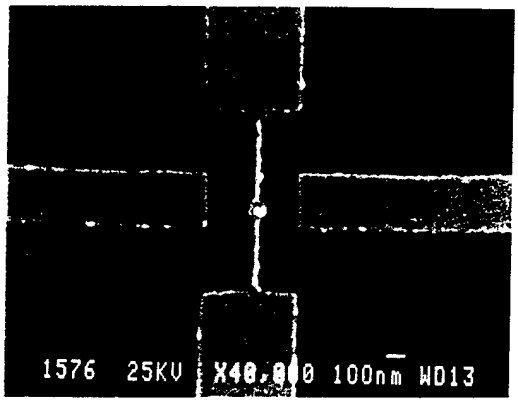
The new QDT has a nanoscale dot-gate placed inside the gap of a split gate. Both gates are on top of a heterostructure [Fig. 1(a)]. The dot gate, which consists of a dot at the middle of a wire, is positively biased to induce a QD and two one-dimensional (1D) wires at the heterostructure interface. The wires connect the dot to the two-dimensional electron gas (2DEG) at the source and the drain. The split gate is negatively biased to change the number of electrons inside the dot and to make the confinement potential stronger. For a given positive dot-gate bias, the electric field beneath the dot is larger than that beneath the wires, therefore the conduction band edge under the dot is lower than that under the wires, creating a quantum dot attached to two wires.

The edge of the first 1D subband in the wire can be controlled by the gate voltage to be above or below the Fermi level of the 2DEG. In the first case, the two wires act like potential barriers that separate the QD from the source and drain. Scanning the dot gate or the split gate will move the energy levels in the dot up or down with respect to the Fermi level. When an energy level inside the dot lines up with the Fermi level, resonant tunneling of electrons from the source to the drain occurs. In the second case, the QD is connected to the source and drain by two 1D channels, new phenomena due to quantum interference will manifest. In this letter, we only discuss the first case. The second case will be reported elsewhere.[7]

Figure 1(b) shows scanning electron micrograph of a typical gate structure: a dot gate has a dot of 80 nm diam in the middle of a 30 nm wide metal wire, and the split gate has a gap of 0.5 μm and a gate length of 0.3 μm. The gates were fabricated on top of a δ-doped AlGaAs/GaAs heterostructure using e-beam lithography followed by a liftoff of Ti/Au.[8] The heterostructure was grown by molecular beam epitaxy and has a 40 nm distance between the gate metal and the 2DEG. At 77 K in the dark, the 2DEG has an electron concentration of 3.5×10^{11} cm^{-2} and a Hall mobility of 90 000 cm^2/V s.



(a)



(b)

FIG. 1. (a) Schematics, (b) scanning electron micrograph of a field-induced quantum dot transistor that has a dot gate inside the gap of a split gate. The dot gate has an 80 nm diam metal dot in the middle of a 30-nm-wide metal wire.

 0003-6951/93/63(16)/2257/3/$6.00

Superlattice & Microstructure
~~Appl. Phys. Lett.~~ ~~Ms. #L-7680~~
J-39
Ref-4

Effects of Bias and Temperature on One-Dimensional Ballistic Transport in a Planar Double-Gate Quantum Wire Transistor

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The combined effects of bias and temperature on one-dimensional ballistic transport in a planar double-gate quantum wire transistor are investigated. A simple formula that quantitatively describes both effects is derived and found to fit experiments well. Other energy broadening factors are found to be significant. Furthermore, due to the strong confinement potential in the device, the current quantization is still observable at a temperature up to 26 K or with a drain bias up to 12 mV.

PACS numbers: 72.10.Bg, 73.20.Dx, 73.40.Kp

Quantum wave bandstop filters

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Ref -5

(Received 3 May 1994; accepted for publication 12 August 1994)

We propose and demonstrate, based on the concept of a microwave bandstop filter, two quantum wave bandstop filter structures. Both structures employ nanoscale gates in a heterojunction transistor to induce a quantum cavity connected by two one-dimensional wires. As the electron wavelength is changed by the gate voltage, we observed that, at certain gate voltages, the transmission of electron waves through the cavity is partially blocked and the drain current drops as large as 50%. This phenomenon is explained in terms of the destructive quantum interference between different electron wave modes in the cavity. © *1994 American Institute of Physics.*

Because of the similarity between electron waves in a quantum waveguide and electromagnetic waves in a microwave waveguide, many microwave device concepts can be instructive in engineering new high functionality quantum devices.[1] Previously, several structures based on such analogy have been proposed and discussed.[2–8] Examples are a stub-tuning device,[2–5] a double-bend quantum waveguide,[6] and a cavity coupled to two quantum waveguides.[6–8] However, most of these studies were limited to the computer simulations and theoretical analysis. Experimentally, only in stub-tuning devices, weak conductance modulations as a function of gate voltage were observed and attributed to the quantum interference effect.[4,5] Here we propose and demonstrate, based on the concept of a microwave waveguide cavity bandstop filter, two quantum wave bandstop filter structures consisting of field-induced nanoscale cavities and one-dimensional (1D) wires. As the electron wavelength is changed by the gate voltage, we observed that, at certain gate voltages, the transmission of electron waves is partially blocked and the drain current drops drastically. This phenomenon is explained in terms of the destructive interference between different electron wave modes in the cavity.

The quantum wave filters employ two different types of nanoscale gate structures on top of a heterostructure to induce, using field effects, a quantum cavity connected by two 1D wires. The first type has a dot gate inside the gap of a split gate [Fig. 1(a)]. The dot gate has an 80-nm-diam metal dot in the middle of a 30-nm-wide metal wire. When positively biased, the dot gate induces, at the heterostructure interface underneath the gate, a nanoscale electron cavity connected by two 1D wires. The negatively biased split gate controls the electron population in the cavity and wire, and also improves the electron confinement.[9] Since the cavity is primarily defined by the positive bias on the dot gate, it is called an enhancement mode cavity.

The second type of gate structure has a straight wire gate between a pair of U-shape split gates [Fig. 1(b)]. The negatively biased U-shape split gate depletes the electron underneath it and thus defines the cavity. The lithographic dimension of the cavity is 0.3 μm×0.5 μm, the actual dimension of confinement at the heterostructure interface can be much smaller due to finite depletion width. The wire gate is positively biased to separately control the electron population in the cavity.[10] In this case, the cavity is primarily defined by the negative bias on the split gate, it is called a depletion mode cavity.

In both structures, the quantum cavity is coupled to the two-dimensional electron gas (2DEG) reservoirs on both sides through 1D wires (quantum waveguides). If the Fermi level is below the threshold of the first subband in the 1D waveguides, the 1D waveguides become barriers, and the electron transport through the structure is in tunneling regime. If the Fermi level is above the threshold of the first subband in the 1D waveguides, the electron wave can propagate through the waveguides, and the transport is in propagation regime. In this experiment, we focus on the propagation regime and study the case where only a single incident mode exists in the 1D waveguide.

The gate structures are fabricated on top of a δ-doped AlGaAs/GaAs heterostructure using electron-beam lithography followed by a lift-off of Ti/Au. The heterostructure consists of a 0.5 μm GaAs buffer layer on a semi-insulating GaAs substrate, a 20 nm undoped $Al_{0.3}Ga_{0.7}As$ spacer layer, a δ-doped layer with a Si concentration of 7×10^{12} cm^{-2}, a 15 nm undoped $Al_{0.3}Ga_{0.7}As$ layer, and a 5 nm n-GaAs cap layer with a Si concentration of 3×10^{18} cm^{-3}. The distance between the gate metal and the 2DEG is 40 nm. At 4.2 K in the dark, the 2DEG has a mean free path of 2 μm.

The characteristic of both devices are measured at T=0.5 K in a He^3 sorption pumped refrigerator. For the enhancement mode cavity device, the split-gate voltage is fixed

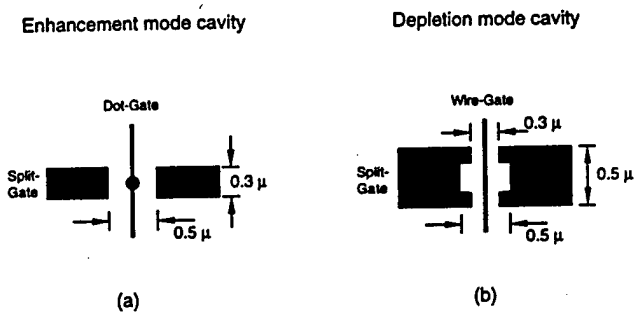

FIG. 1. Schematic diagram of the gate structures used to create a cavity coupled to two 1D waveguides. (a) An enhancement mode cavity: cavity induced by the positive bias on the dot gate. (b) A depletion mode cavity: cavity created by negative bias on the U-shape split gate.

 0003-6951/94/65(16)/2072/3/$6.00

Superlattices and Microstructures, Vol. 17, No. 2, 1995

Ref-693

ELECTRON TRANSPORT THROUGH A QUANTUM CAVITY

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(Received 10 January 1995)

Electron transport through a quantum cavity coupled with two one-dimensional waveguides is studied using a generalized scattering matrix method. In a symmetric *N*-channel cavity model, we are able to obtain an exact solution that predicts the electron energies at which the transmission of electron waves become zero. We found that the zero of transmission is closely related to the longitudinal resonance through inter-channel scattering, in particular, to the resonance of the highest propagating mode inside the cavity. This model provides a simple way to calculate the electron transmission through a cavity which could be useful in quantum waveguide engineering.

1. Introduction

Electron transport through coupled quantum waveguides show interesting interference patterns.[1] Previously, various types of waveguide structures, such as a cavity,[2-4] T-shape stub[5-7] or double bend,[2] were investigated, mostly by computer simulations. Here, we perform an analytical study of the electron transmission through a quantum cavity coupled with two one-dimensional waveguides using a generalized scattering matrix method. In a symmetric *N*-channel cavity model, we are able to obtain an exact solution that predicts the electron energies at which the transmission of electron waves become zero. We will show that the zero transmission is closely related to the longitudinal resonance and inter-mode scattering inside the cavity. The model provides a simple way to calculate the electron transmission through a cavity which could be useful in quantum waveguide engineering.

2. Model

To establish the model, let us consider a rectangular cavity coupled to two identical one-dimensional (1D) waveguides (leads) as depicted in Fig. 1(a). We make three simplifications. First, we adopt the standard hard wall approximation, thus the threshold energy of each lateral mode is simply $\varepsilon_n^{(i)} = \hbar^2/2m^* (n\pi/w_i)^2$, where m^* is the effective mass of an electron, n is the mode index, w_i is the width in the ith region, and i = I, II denotes the leads and the cavity, respectively. Second, we neglect all the evanescent waves in the cavity which decay exponentially with the cavity length, L. In exact numerical calculations, the evanescent waves are necessary since they contribute significantly to the boundary matching. But in our S-matrix treatment, the effects of the evanescent waves can be largely taken into account by a rescaling of the matrix elements.[8]

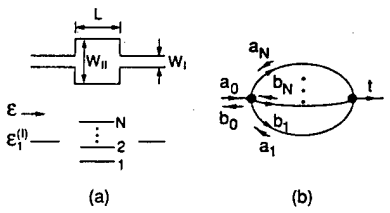

Fig. 1 (a) A rectangular cavity coupled to two identical 1D leads. Only one propagating mode exists in the leads, but there are *N* propagating modes inside the cavity. (b) In this model, all evanescent waves are neglected, therefore the cavity is equivalent to *N* thin wires joined together at two ends.

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Observation of quantum effects and Coulomb blockade in silicon quantum-dot transistors at temperatures over 100 K

Ref-7

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(Received 21 March 1995; accepted for publication 15 June 1995)

We report the fabrication and characterization of lithographically defined nanoscale silicon quantum-dot transistors that operate at temperatures over 100 K and a bias higher than 0.07 V. In the tunneling regime, these transistors show strong current oscillations due to quantum confinement and single-electron charging effects. In the propagating regime, a different kind of current modulation has been observed, which is attributed to the interference between different modes of quantum waves in a cavity. Proper scaling of these transistors should lead to operation at room temperature and a bias of 0.3 V. © *1995 American Institute of Physics.*

Quantum and single electron charging effects are bringing new functionalities into transistors. The new transistors can reduce the number of transistors per circuit function and open up opportunities for innovative architectures.[1,2] However, in field effect transistors, manifestation of quantum effects and single-electron Coulomb blockade usually requires extremely low temperatures such as sub-liquid helium temperatures. Furthermore, the quantum effect and Coulomb blockade transistors are typically fabricated in III–V compound semiconductors instead of Si—the backbone material of the integrated circuit (IC) industry. To make the quantum effects and single-electron Coulomb blockade transistors practical for circuits application, the room-temperature operation and made-in-silicon are essential. This can be achieved if the silicon transistors have a feature size of about 10 nm. Here, we report the fabrication and characterization of lithographically defined nanoscale silicon quantum-dot transistors (QDT) that demonstrate quantum effects as well as single electron Coulomb blockade at temperatures over 100 K. They are also the first Si transistor that shows interference between different modes of quantum waves in a cavity. Proper scaling of such quantum-dot transistors should lead to room-temperature operation.

As shown in Fig. 1, the transistors were fabricated on (100) SIMOX (separation by implanted oxygen) silicon wafers with the top silicon layer of 60 nm thick. The channel, having an abacus bead shape, was etched into the top Si layer with chlorine based RIE (reactive ion etching) after EBL (*e*-beam lithography). PMMA (polymethylmethacrylate) resist was used for the EBL. The bead defines the quantum dot which is connected to the source and the drain through two constrictions. The channel has a similar shape as that of the QDT in III–V compound semiconductors.[3] By using *e*-beam lithography instead of stress dependent oxidation to define the quantum dot,[4] the size and shape of the dot can be better controlled. Following the 400 Å gate oxide growth at 1000 °C, which reduced the size of the silicon quantum dot and constrictions, a rectangular plain polysilicon gate was fabricated to cover the entire abacus bead channel. The high-temperature oxidation also annealed any damages that occurred during RIE. QDTs with various sizes were fabricated; the smallest Si dot diameter achieved after oxidation is estimated to be 20 nm from the scanning electron microscopy (SEM) pictures.

The transistors have two operation regimes. First is the tunneling regime. When the gate voltage is not significantly larger than the transistor's threshold voltage, the Fermi level is below the potential barriers of the double constrictions. Thus the silicon quantum dot is separated from the source and the drain by two potential barriers, and the source-drain current is due to tunneling through the discrete levels in the quantum dot. The other is the propagation regime. When the gate voltage is sufficiently higher than the threshold voltage, the Fermi level is pushed above the potential barriers that separate the quantum dot from the source and the drain. Electron waves can then propagate through the entire channel without tunneling. In this case, the quantum dot acts like a cavity in a waveguide, which will cause conductance variations due to wave interference effect.

The transistors were measured in a chamber in which the

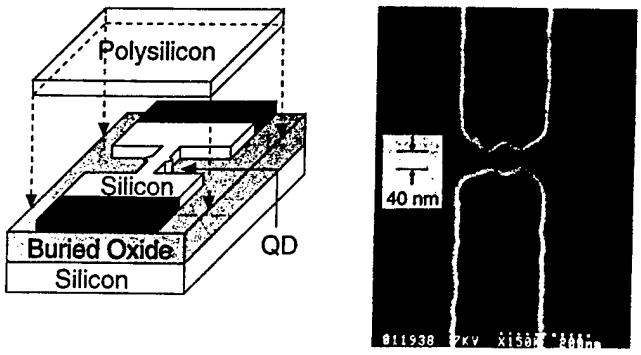

FIG. 1. (a) Schematic of a Si quantum-dot transistor where the channel having an abacus bead shape was etched into the top Si layer of a SIMOX wafer. The bead defines the quantum dot that is connected to the source and drain through two constrictions. The rectangular polySi gate covers the entire quantum dot (QD). (b) SEM micrograph of the abacus bead channel etched into the top Si layer before oxidation. The dot size and the constriction width are further reduced during the gate oxide growth at high temperature.

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 0003-6951/95/67(7)/938/3/$6.00

Single hole quantum dot transistors in silicon

Ref-8

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(Received 3 May 1995; accepted for publication 8 August 1995)

Novel *p*-channel quantum-dot transistors were fabricated in silicon-on-insulator. Strong oscillations in the drain current as a function of the gate voltage have been observed at temperatures over 81 K and drain biases over 66 mV. The oscillations are attributed to holes tunneling through the discrete single hole energy levels in the quantum dot. Measurements show that the average energy level spacing is ~35 meV. Simple modeling indicates that about two thirds of the energy level spacing come from the Coulomb interaction between holes (i.e., hole Coulomb blockade) and one third from the quantum confinement effect. The realization of single hole quantum-dot transistors opens new possibilities for innovative circuits that utilize complementary pairs of quantum-dot transistors. © *1995 American Institute of Physics.*

In exploring the limits of semiconductor transistors and searching for innovative devices, several electron quantum-dot transistors in silicon have been demonstrated.[1-3] The strong oscillation in the drain current is due to interplay between the quantum confinement effect and Coulomb blockade effect of electrons.[2] The possibility of hole Coulomb blockade has been speculated for some time,[4] however, it has not been demonstrated in any transistor albeit some studies on hole effects in Si–SiGe diodes.[5,6] Here, we report novel *p*-channel quantum-dot transistors in silicon that have shown single hole Coulomb blockade as well as hole quantum size effect at temperatures over 81 K.

The *p*-channel quantum-dot transistors were fabricated on a silicon-on-insulator (SOI) wafer that was made using separation by implanted oxygen (SIMOX). The top silicon thickness is 70 nm and has a boron concentration of 3×10^{15} cm^{-3}. However, as shown later, the quantum dot is virtually undoped due to its extremely small dimensions. In fabrication, the quantum dot with an abacus bead shape was first etched into the top silicon layer, using electron beam lithography and reactive ion etching, as shown in Fig. 1. It was followed by oxidation of 41 nm thick gate oxide, and deposition and patterning of a rectangular polycrystalline silicon gate to cover the entire quantum dot and constrictions as seen in Fig. 1. The fabrication process is identical to that of the electron quantum-dot transistors in silicon,[2] except that the source, the drain, and the polycrystalline silicon gate were doped with BF_2 implantation. After the fabrication, the actual size of the silicon bead was studied by etching away the gate oxide in diluted HF and was found to be ~10 nm wide, 30 nm long, and 30 nm thick (Fig. 2). The average dopant inside the quantum dot can then be calculated by multiplying the quantum dot volume with the average doping concentration which becomes 0.03 dopant per quantum dot. In other words, the quantum dots are virtually undoped and the effects observed in the transistors have nothing to do with the dopants in the channel.

The *p*-channel quantum-dot transistors were measured in dc with an HP4145B and in a variable temperature chamber. The gate was biased negatively, inducing holes in the quantum dot channel, while the drain was biased negatively to drive holes from the source to the drain. As the gate voltage was scanned, the drain current (i.e., the hole current) oscillated (Fig. 3). The oscillation is due to holes tunneling through the discrete single hole energy levels in the quantum dot. The current peaks when the Fermi level in the source is aligned with a single hole energy level in the quantum dot. The current valleys when the Fermi level is in between two hole energy levels. Since the hole current oscillation persists at temperatures over 81 K and thermal broadening is about $4k_BT$, where k_B is the Boltzman constant and T is the temperature, the average hole energy level spacing in the quantum dot is estimated to be over 30 meV. The energy level spacing can also be estimated from the temperature dependent study of the thermal activation of the valley current,[7] from which we found the energy level spacing to be 33 meV in agreement with the thermal broadening study.

The drain bias effect on the oscillation is shown in Fig. 4. Due to the large energy level spacing, the ratio of the peak to valley current at 1 mV drain bias can be well over 10 000, and the oscillation can be clearly observed at a drain bias over 66 mV.

The hole QDTs with a variety of quantum-dot sizes were fabricated. It has been observed that the operating temperatures as well as the peak-to-valley current ratio depend on the

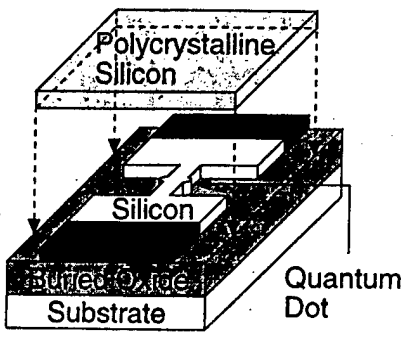

FIG. 1. Schematic of the single hole transistors with the quantum dot separated from the source and drain by two constrictions. The polycrystalline silicon covers the entire quantum dot.

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 0003-6951/95/67(16)/2338/3/$6.00

Single electron and hole quantum dot transistors operating above 110 K

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Ref-9

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Both single electron and hole quantum dot transistors in silicon-on-insulator were fabricated and characterized. The quantum dots were formed using electron-beam nanolithography and reactive ion etching. The single electron quantum dot transistors show the oscillation of the drain current as a function of the gate voltage at temperatures up to 170 K and drain biases up to 80 mV. The oscillation is due to electron tunneling through the discrete energy levels inside the quantum dot. The average energy level spacing is ~60 meV. Data analysis shows that the discrete energy levels are caused by Coulomb interaction as well as quantum size effects. The single hole quantum dot transistors show similar oscillations up to 110 K and drain biases up to 50 mV. The average energy level spacing is ~36 meV. © *1995 American Vacuum Society.*

I. INTRODUCTION

Until recently, quantum dot transistors (QDTs) have been primarily based on GaAs–AlGaAs heterojunction and the electric field-induced confinement.[1] However, the electric field-induced confinement cannot create a quantum dot small enough to permit high operation temperatures. With the recent advancement in silicon-on-insulator (SOI) wafers, particularly separation by implanted oxygen (SIMOX) wafer technology, it is now possible to use silicon dioxide to form very small quantum dots with excellent confinement.[2–4]

We have developed a new method of fabricating QDTs on SIMOX using electron-beam lithography (EBL) and reactive ion etching (RIE). By using EBL instead of the stress-dependent oxidation rate to define the quantum dots[3] the sizes and shapes of the quantum dots could be better controlled. Using this method, we have fabricated single electron and single hole silicon QDTs that can operate above 110 K. The possibility of single hole QDTs have been speculated for some time;[5] however, they were not demonstrated in any three terminal devices except for some studies on hole Coulomb blockades in Si–SiGe two terminal diodes.[6,7] In this paper, we present the fabrication process of both single electron and single hole QDTs in silicon and compare their characteristics.

II. DEVICE STRUCTURE

As shown in Fig. 1, the silicon QDT consists of a quantum dot separated from the source and the drain by two constrictions. The quantum dot is surrounded by thermal oxide and has a gate on top that can change the charge concentration inside the dot. Since the quantum dot is small, discrete energy levels will be formed. The constrictions with a size smaller than that of the quantum dot create the tunneling barriers: one is between the quantum dot and the source and the other is between the quantum dot and the drain. The source and the drain were doped n-type for electron QDTs and p-type for hole QDTs. For single electron QDTs, the gate and drain voltage are positive to induce electrons in the quantum dot and to drive the electrons from the source to the drain. For hole QDTs, the two biases are reversed. When one of the discrete energy levels inside the dot is aligned with the Fermi level at the source, charge can tunnel through the barriers, giving resonant tunneling current. The resonance and off-resonance in the tunneling lead to the drain current oscillating with the charge population in the quantum dot, and therefore with the gate voltage.

III. FABRICATION

The starting SIMOX wafer has a 360-nm-thick buried oxide and 60-nm-thick top silicon layer. A 30-nm-thick sacrificial oxide was grown first and optical lithography was used to pattern the oxide for the active area as shown in Fig. 2. EBL was used to pattern the quantum dot with polymethymethacrylate (PMMA) resist. The pattern on PMMA was then transferred to the sacrificial oxide layer which in turn was transferred to the top silicon layer using RIE as shown in Fig. 2. After the removal of the sacrificial oxide mask, the gate oxidation was performed followed by the deposition and patterning of undoped polysilicon to cover the whole quantum dot. This was followed by self-aligned source drain implantation. For the electron QDTs, phosphorus implantation with dose of 2×10^{15} cm^{-2} and energy of 40 keV was used, while BF_2^+ implantation with dose of 2×10^{15} cm^{-2} and energy of 70 keV was used for the hole QDTs. The final anneal to activate the dopant was done at 950 °C in a regular fur-

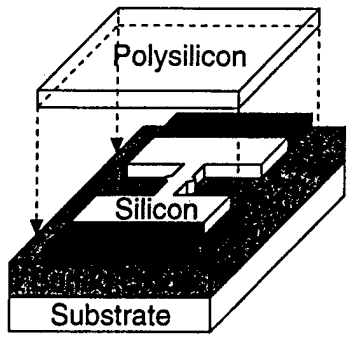

FIG. 1. Schematic of a silicon quantum dot transistor with quantum dot separated from the source and drain by the two constrictions. For clear illustration, the gate is lifted and the gate oxide is not shown.